Nanowire transistors, lasers and hetero-engineering

Semiconductor nanowires constitute a growing field of research, particularly as the size of commercial devices decrease. Dr Mike Cooke looks at some recent research looking to achieve ultra-small transistors, photovoltaic devices, lasers and bandgap engineering.

The focus in the mainstream semiconductor has been on the nano-scale for some time. As this research and development progresses, the challenges are certainly immense, but also new opportunities come in view. In addition to research aimed at characterizing CMOS structures and interconnection wires with nano-scale dimensions, there are hopes of using semiconductor nanowires for transistor channels, single-electron memory, nanoelectrodes, photonics (light/laser production, sensing), and energy conversion (battery and photovoltaic). Scientific activities include fundamental electron transport studies, and chemical and biological sensing and manipulation. Here we focus on recent attempts to produce transistors, photovoltaic devices, lasers and heterostructures in various materials.

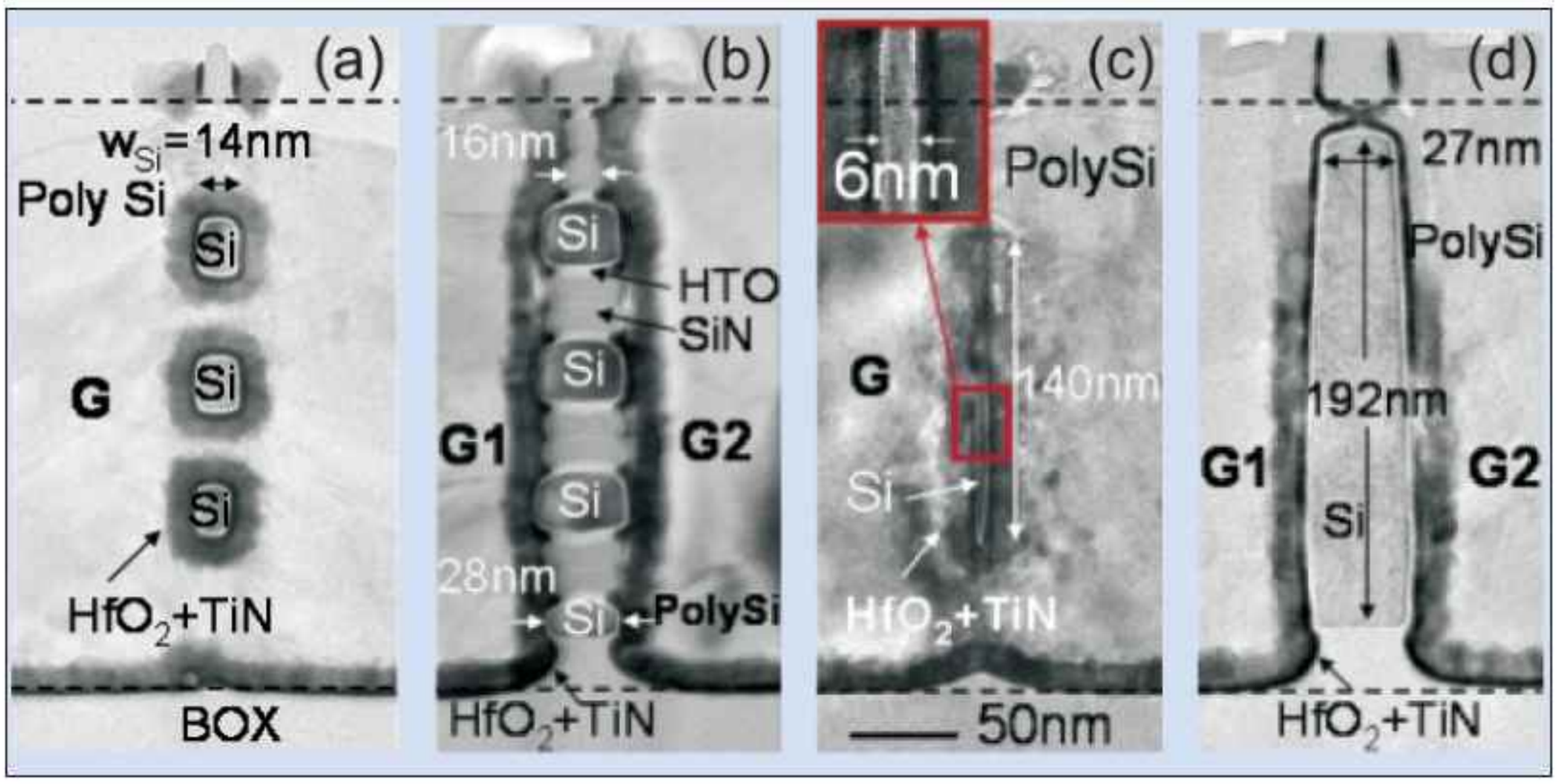

Figure 1. Different nanowire and FinFET structures produced on SOI wafer with HfO_2 TiN poly-Si gate stack: (a) 3D-NWFET; (b) ΦFET; (c) FinFET; (d) IG-FinFET. The distance between the dotted lines is 250nm.

Transistors

CEA-LETI has integrated on one silicon-on-insulator wafer different advanced transistor structures to test the capabilities of stacked nanowire transistors (3DNWFET, Figure 1). Adding an optional independent gate structure creates a device called a ΦFET (Figure 2).

These structures involve sub-15nm diameter nanowires being stacked in 3D configurations using a 'FinFET-like CMOS technology'. When the SiGe is etched away from alternating superlattice layers of Si and SiGe, multiple silicon nanowire channels remain. Gates are then wrapped around each individual nanowire. A high-k dielectric/metal gate electrode stack is used.

The process technology consisted of a common flow compatible with standard planar fully depleted (FDSOI) devices that are due to come to prominence in the next decade as device sizes shrink according to the

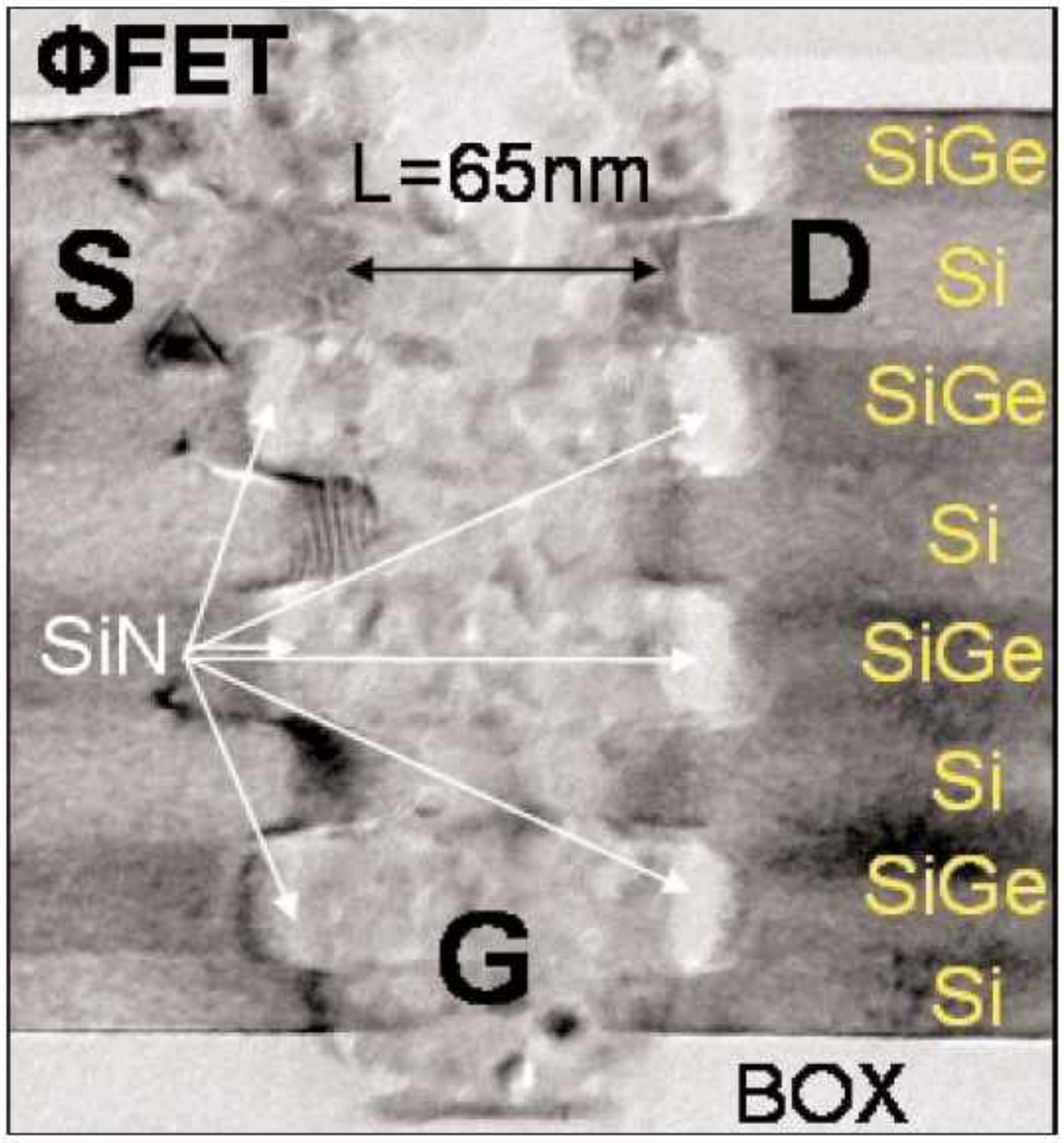

Figure 2. ΦFET in more detail.

International Technology Roadmap for Semiconductors. The devices were processed within CEA-LETI facilities using electron-beam lithography capable of producing 15nm gate-length devices.

FinFETs and independent-gate FinFETs (IG-FinFETs) were co-processed on the same wafer for comparison purposes. The ability to combine different device structures on the same chip also allows optimization of performance, density and power consumption.

Drive currents of 6.5mA/μm for NMOS and 3.3mA/μm for PMOS 3DNWFETs are described as 'extremely high'. The 3DNWFET channel width needed for a given drain-induced barrier lowering is relaxed by a factor of 2.5 compared with the FinFET (i.e. the 3DNWFET can be 2.5 times narrower, allowing further technology compression). Other transport properties are also improved.

The ΦFET also showed significant enhancement compared with IG-FinFETs: the off current is two decades smaller, and the sub-threshold slope is also smaller, at 82mV/dec compared with 95mV/dec.

Full results showing the structures and the electrical results were presented at December's IEEE International Electron Devices Meeting (IEDM 2008) [1]. The work was carried out in the frame of the French Carnot Institutes initiative and in collaboration with IMEP Grenoble and STMicroelectronics Crolles, France.

A whole session at IEDM [2] was devoted to other approaches to silicon nanowire transistors along with a number of additional SiNWFET presentations outside this session. Other nanowire research at IEDM included silicon nanowire use in drug delivery systems, biological sensing and battery anodes, and one group described low-power, high-speed InSb nanowire FETs.

Photovoltaics

Silicon nanowires are also the basis of two approaches to photovoltaic devices. University of California Berkeley researchers Erik C. Garnett and Peidong Yang see vertically aligned silicon nanowires as a route to lower-cost photovoltaic devices [3]. This is based on there being less need for ultra-purity in the initial substrate compared with planar silicon photovoltaic devices.

The Berkeley silicon nanowire arrays are produced using a solution phase etch on an n-type substrate. A p-type amorphous silicon shell is then deposited on this core using low-pressure chemical vapor deposition (LPCVD). The shell is then crystallized by using a rapid thermal anneal (RTA) step (1000°C for 10 seconds in forming gas).

Although the efficiency of the resulting cells (Figure 3) was only 0.5%, Garnett and Yang believe that they can develop cells with efficiencies close to that of bulk silicon devices. The nanowires are about 18μm in length and cover about 50% of the area of the wafer. The core has a diameter of the order of 50–100nm and the shell is

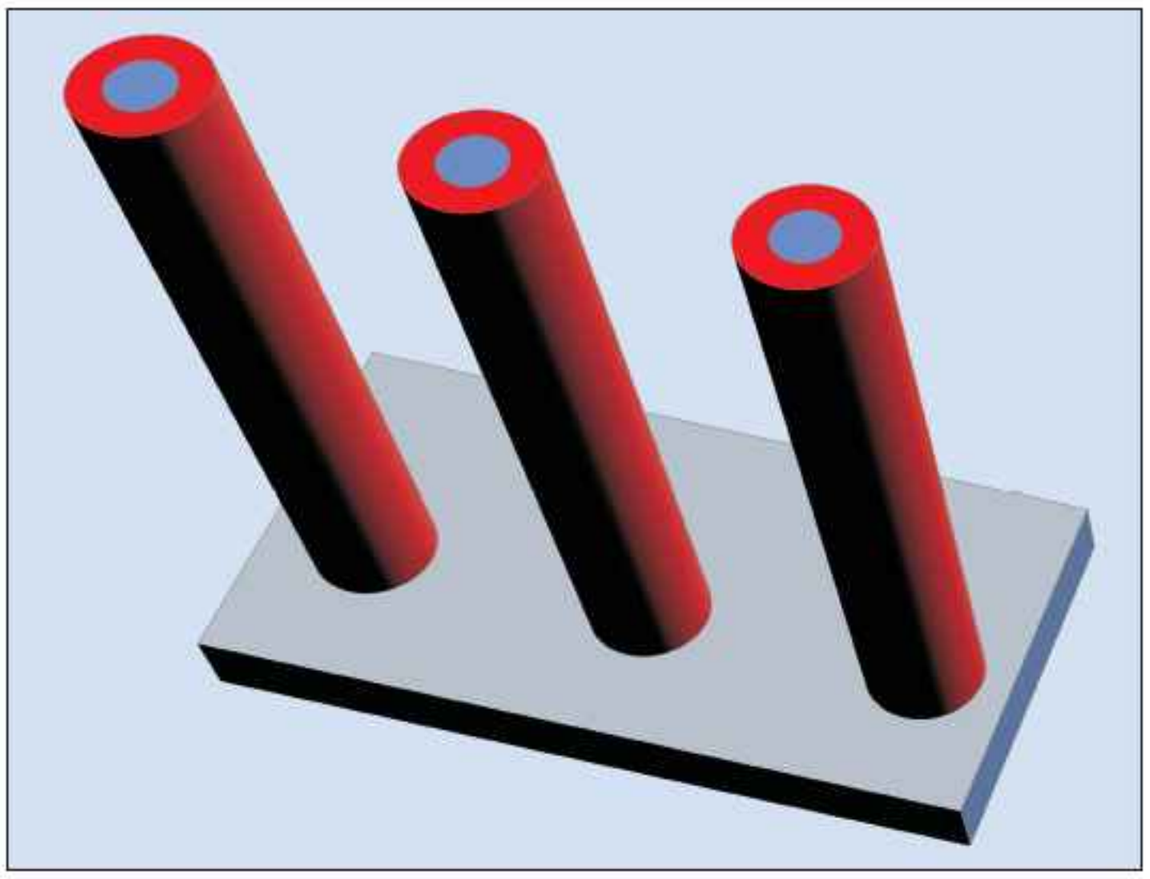

Figure 3. Schematic of Berkeley's vertical nanowire photovoltaic array.

150nm thick to give a total diameter of 350–400nm. The array was tested under AM1.5 conditions (air mass 1.5 solar illumination at zenith angle ~49°, typical of northern hemisphere conditions for the USA and EU). The open-circuit voltage (V_{OC}) was 0.29V and the short-circuit current (J_{SC}) was 4.28mA. The fill factor (maximum power/(V_{OC}xJ_{SC})) is 0.33. The overall efficiency is 0.46%.

The nanowire's high ratio of surface area to volume exacerbates unwanted recombination at interfaces, reducing V_{OC} and hence the efficiency. One route to higher efficiency is believed to be through improving the surface passivation. Other ideas include reducing the surface roughness of the wires and increasing the p-Si conductivity to reduce series resistance. Concern is also expressed about the quality of the contacts.

Rather than producing the p-n junction in a radial direction, Harvard and Stanford universities [4] have produced axial modulation-doped p-i-n and tandem p-i-n^+-p^+-i-n silicon nanowire photovoltaic elements (i.e. the doped elements are ordered along the wire). The diameters of the wires were in the range 200–250nm (Figure 4). AM1.5 testing gave a V_{OC} of 0.29V, J_{SC} of 3.5mA/cm^2 and 0.5% maximum efficiency for an optimized p-i-n structure. The maximum power output was found to be 4.6pW. This increases to 31pW under illumination of 4.5 suns, which could be arranged under light concentrator conditions.

Performance increases with the length of the undoped intrinsic region (0, 2 and 4μm lengths were studied). One effect of the increased length of undoped material is to reduce the saturation current of the diode and hence the leakage current when operating as a photovoltaic device.

The tandem arrangement with a 2μm i-region in each section increased V_{OC} by 57% to about 0.36V over the 0.23V for the comparable 2μm single device. The

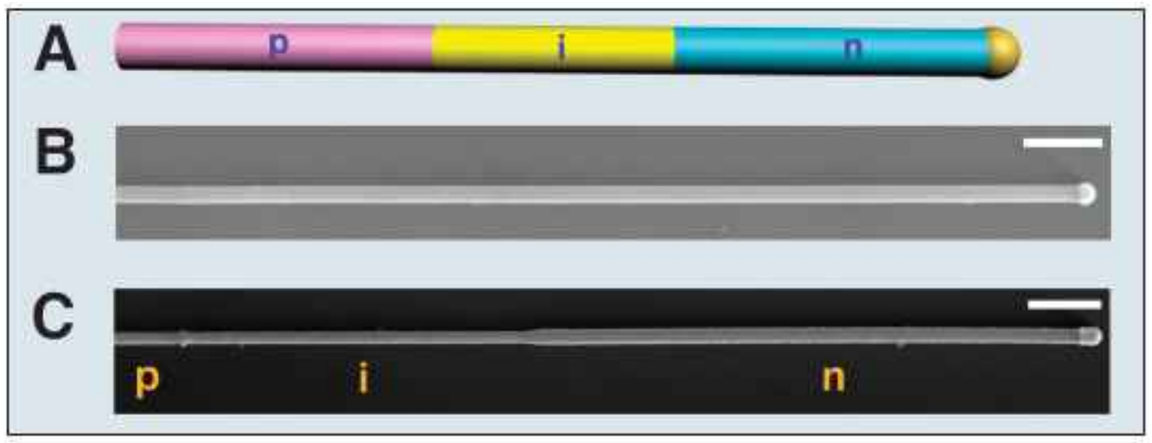

Figure 4. Axial p-i-n Si NWs scheme (A), and SEMs before (B) and after a selective wet etching process (C) that shows p and i regions due to faster etch rate.

power increased 39% from 2.3pW to 3.2pW. Ideally, the tandem arrangement should have given a 100% increase in power. The difference is attributed to parasitic resistances, particularly at the n^+-p^+ tunneling interface between the diodes.

A gold nanoparticle catalyst was used to produce the nanowires using a vapor–liquid–solid (VLS) growth method. The length of the unintentionally doped (i) section was varied to enable tuning of the device properties. The doping was achieved by using different dopant precursors (p from boron, n from phosphorus) at various stages.

The values for V_{OC} in both axial and coaxial/radial geometries are about half that found in polycrystalline planar devices (0.6–0.7V). The similarity of the V_{OC} values suggests that the mechanism for suppression from planar levels may be related. Harvard also produced coaxial p-i-n silicon nanowire photovoltaic devices in 2007 and reported maximum power outputs of 200pW and apparent efficiencies of 3.4% [5]. The wires were produced by similar VLS methods.

Charles M Lieber, principle investigator at Harvard, comments: "Our radial and axial device studies illustrate how structure (axial versus radial p-n junction) and material (single-crystal versus nano-crystal silicon) affect the fundamental parameters of V_{OC} and J_{SC} in nanowire solar cells. The efficiency of the radial device is higher than that of the axial device, because the former has more efficient carrier separation and light absorption processes that lead to larger J_{SC}. Both single p-i-n junction devices have a similar V_{OC}. The axial device is a nano-scale analog of a planar single-crystal silicon solar cell geometry and its photogeneration of carriers is limited to a relatively narrow depletion region of the NW around the intrinsic silicon block.

"We want to emphasize that, although the performance of the axial device is smaller than that of the radial device, it is still comparable to or better than other reported nanowire solar cell results... while the radial has been the best of those reported. Moreover, the axial device represents a unique opportunity to integrate multiple junctions on a single nanowire for higher voltage and power output, as we demonstrated for the first time in the work with tandem axial photovoltaic devices [4]."

Multi-quantum well laser

Harvard University also works on III–V nanowires; with Georgia Institute of Technology, it has been developing a nanowire multi-quantum well laser. These researchers have recently reported a MQW core/shell nanowire heterostructure that enables lasing over a range of wavelengths at room temperature [6]. The team has performed MOCVD to grow uniform, dislocation-free layers of InGaN/GaN on a triangular GaN nanowire core (Figure 5). The InGaN well thickness is 1–3nm, and structures with 3, 13 and 26 wells have been grown. The cores are grown on sapphire substrates using a nickel nanocluster as catalyst. The precursors are trimethyl-gallium (TMGa), trimethyl-indium (TMIn) and ammonia (NH_3) with hydrogen carrier gas. The MQW layers are found to be thicker on two of the faces of the triangular core.

Optical excitation produced lasing in the various structures with wavelengths in the range 365–494nm at room temperature. The threshold depends on the number of wells. Below threshold, the emission has a relatively broad spectral range, but above threshold the emission collapses into a series of narrow peaks, indicative of lasing.

A representative 26-well wire had a threshold of ~900kW/cm^2 of pump laser power, above which the narrow emission wavelengths around 438nm have full-widths at half maximum of less than 0.8nm (this value is limited by the spectral resolution of the measurement system). The spacing of the emission lines suggests that longitudinal modes of the nanowire cavity are excited. The lasing wavelength is blue-shifted compared to spontaneous emission — a feature of InGaN laser systems, and that has been attributed to band-filling effects and/or photo-induced screening of the internal fields.

The lasing thresholds of the 26-well structures were about 4–10 times lower than those with 13 wells. The thresholds are comparable to optically pumped traditional planar InGaN MQW lasers, but higher than the best values quoted for GaN nanowire lasers. The researchers attribute the higher threshold for InGaN MQW nanowires to their smaller confinement factors. It is hoped to reduce the threshold in future work.

A contrast with planar InGaN devices is that the threshold is much less dependent on the emission wavelength. Planar devices show an exponential increase in threshold with wavelength. This is believed to be related to the deterioration in material quality as the indium content grows. For the nanowires, the researchers believe that the problem is less severe, since the layers are single crystal and dislocation free.

The Harvard/Georgia group believes that free-standing injection nanolasers based on the technology are possible. This would involve adding p-type AlGaN/GaN shells to the structure. The use of such heterostructures opens

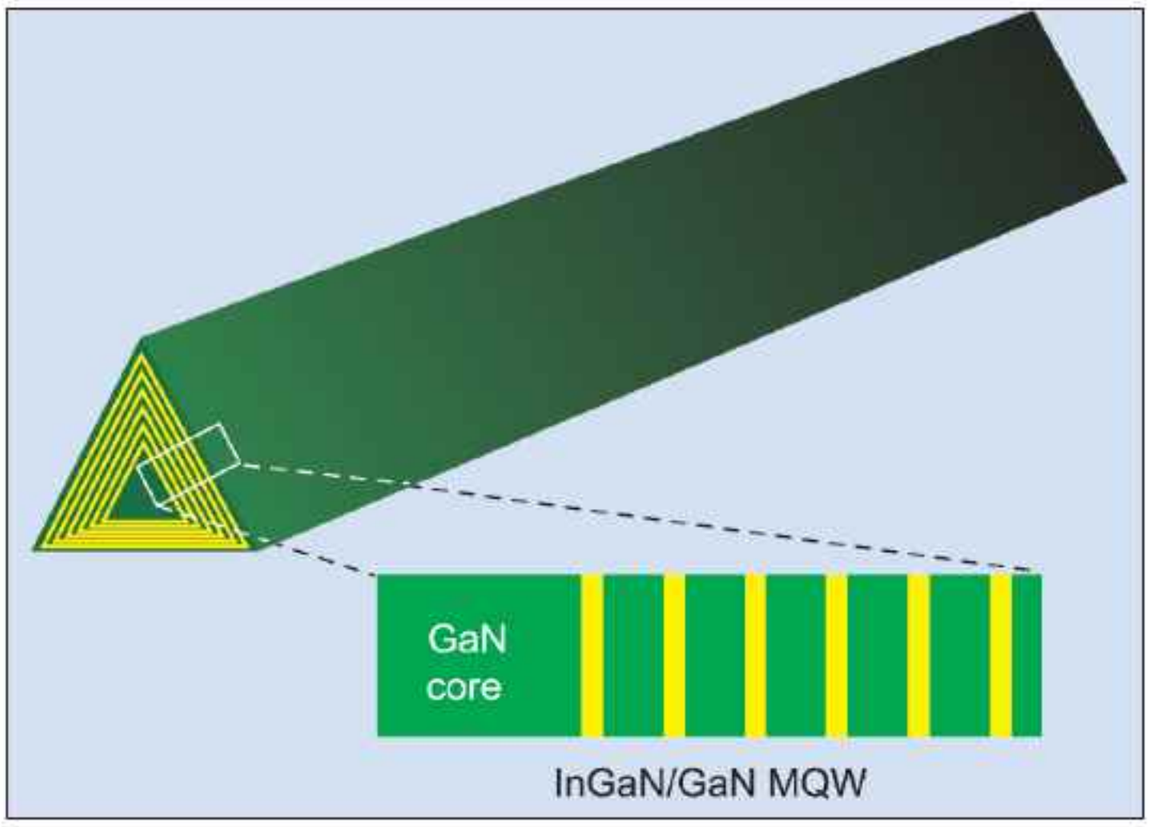

Figure 5. Schematic of GaN nanowire multi-quantum well with triangular cross-section.

up the possibility of engineering the laser wavelength as opposed to the fixed wavelengths of homogeneous compound nanowire lasers previously produced using materials such as GaSb, ZnO, GaN, CdS and ZnS.

Polytype heterostructures

Sweden's Lund University has been studying InAs nanowires. This group has developed a technique to control the crystal structure of such wires [7]. Nanowires made of binary semiconductors, such as InAs, often have a high density of twin defects and stacking faults as they grow. This results in a series of different uncontrollable crystal structures called polytypes. The most common polytypes for InAs nanowires are wurtzite (WZ) and zinc-blende (ZB).

The uncontrollable nature of the change of polytype affects the optical and charge-carrier transport properties of the resulting nanowires. The results can be negative, such as scattering from the fault boundaries increasing resistance to current flow. However, such effects, if they can be controlled, could also lead to new structures and devices based on bandgap engineering. The band offset between the WZ and ZB structures is several tens of meV. In fact, one result of the new WZ–ZB nanowire structures could be a more accurate determination of this offset.

Control over the structure is achieved by varying the size of the gold seed particle and the growth temperature. Smaller-diameter nanowires are largely WZ, moving over to ZB as the diameter increases. Nanowires with diameters of 24nm grown at 460°C had the WZ structure with a stacking fault density of 2 to 3 per micron. Under the same growth conditions, 110nm diameter wires were ZB and had less than 1 fault/micron. Growth at 420°C increases the WZ proportion. This enhances the WZ purity at low to medium diameters and creates a large number of twin-plane faults in the ZB phase at larger diameters.

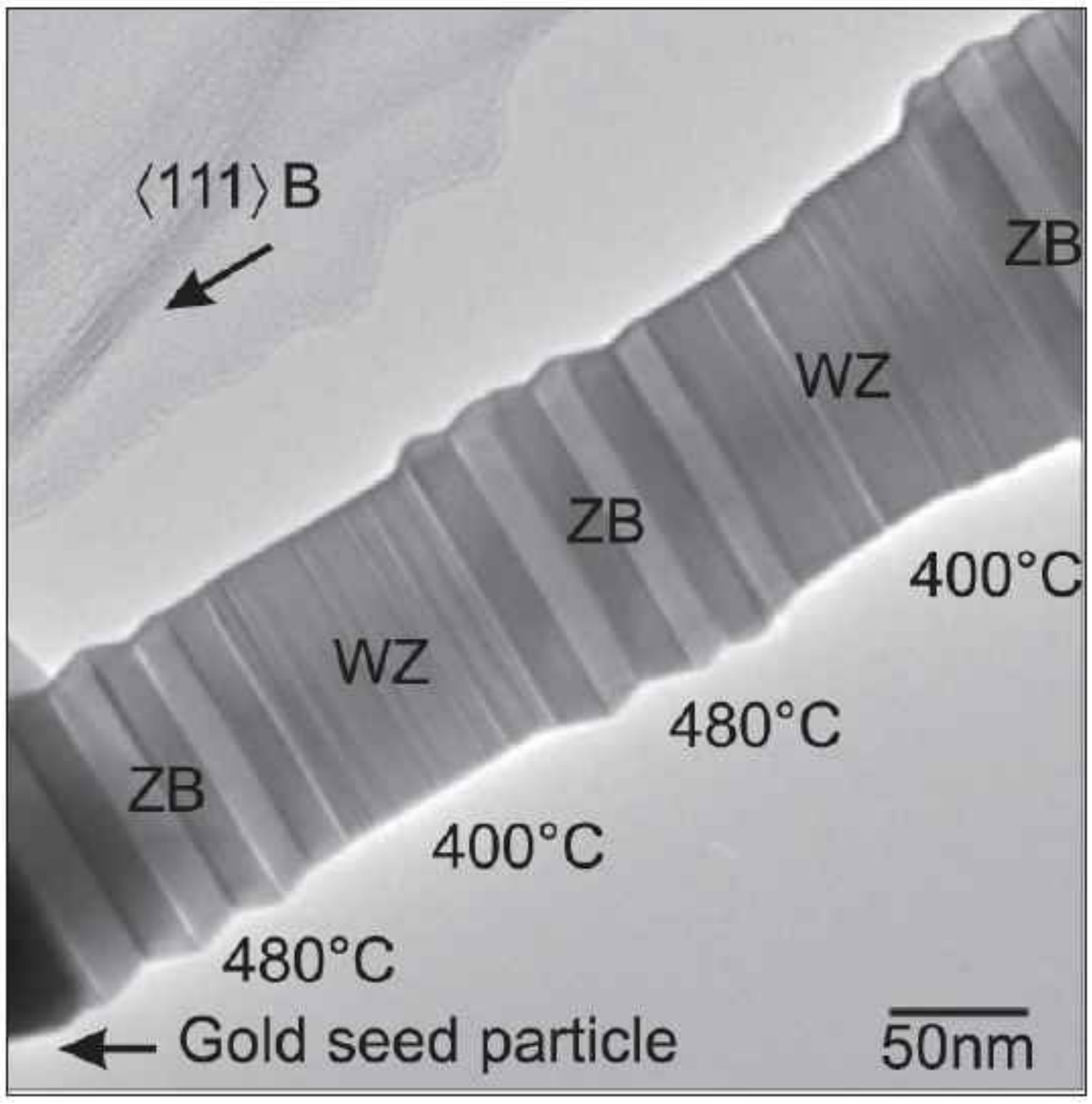

Figure 6. InAs nanowire with different polytypes — wurzite and zinc blende — down its length.

Superlattices consisting of WZ and ZB segments were grown by alternating the growth temperature between 400°C and 480°C (Figure 6). Three ZB segments were separated by WZ. The WZ parts showed some single stacking faults. The researchers believe that this is the result of non-optimal growth conditions, in particular the switching sequence between the temperatures.

The main energy difference between the WZ and ZB polytypes derives from the ionic interaction between third nearest neighbors. Materials with bonds showing a more ionic nature, such as GaN (ionicity 0.557), tend to crystallize as WZ, while lower-ionicity materials like GaSb (0.108/0.246) generally go for the ZB form. Between these extremes come the standard III–V semiconductors such as GaAs, GaP, InAs and InP. The Lund team believes that its methods are applicable to GaAs and InP nanowire growth.

The wires were grown using commercial metal-organic chemical vapor deposition (MOCVD) techniques at a pressure of 10kPa with hydrogen as the carrier gas. The precursors were trimethyl-indium (TMIn) and arsine (AsH_3). The gold particles were deposited on the InAs substrate using a dedicated aerosol system. ■

References

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